**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| Appellant: | Sheu, *et al.* | Docket No.: | TSM03-0140 |
| Serial No.: | 10/619,828 | Art Unit: | 2891 |
| Filed: | July 15, 2003 | Examiner: | Movva, Amar |
| For: | Self-Aligned MOSFET having an Oxide Region below the Channel | | |

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

## APPEAL BRIEF

Dear Sir:

This Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Final rejection mailed May 17, 2007. A Notice of Appeal was filed on September 28, 2007.

## REAL PARTY OF INTEREST (37 C.F.R. 41.37(c)(1)(i))

The real party in interest for this appeal is:

Taiwan Semiconductor Manufacturing Company, Ltd.

## RELATED APPEALS AND INTERFERENCES (37 C.F.R. 41.37(c)(1)(ii))

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

## STATUS OF CLAIMS (37 C.F.R. 41.37(c)(1)(iii))

### *A. Total Number of Claims in Application*

There are 12 claims pending in application.

### *B. Current Status of Claims*

Claims canceled: 0

Claims withdrawn from consideration but not canceled: 0

Claims pending: 1-12

Claims allowed: 0

Claims rejected: 1-12

### *C. Claims On Appeal*

The claims on appeal are claims 1-12

## STATUS OF AMENDMENTS (37 C.F.R. 41.37(c)(1)(iv))

Appellant filed a Response Under 34 C.F.R. § 1.116 on July 7, 2007, in which no amendments were made to the claims. The Examiner rejected Appellant's arguments in an Advisory Action dated August 28, 2007. Appellant filed a Notice of Appeal along with a Request for Pre-Appeal Review on September 28, 2007. The Pre-Appeal review board indicated that the application was to remain under appeal, in a Notice of Panel Decision, dated October 24, 2007. Appellant files this Appeal Brief in response to the review panel's decision upholding the Examiner.

## SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R. 41.37(c)(1)(v))

The following provides a concise explanation of the subject matter defined in each of the claims involved in the appeal, referring to the specification by page and line number and to the drawings by reference characters, as required by 37 C.F.R. § 41.37(c)(1)(v). Each element of the claims is identified by a corresponding reference to the specification and drawings where applicable. Note that the citation to passages in the specification and drawings for each claim element does not imply that the limitations from the specification and drawings should be read into the corresponding claim element.

With regard to claims 1-12, a transistor device (200) that includes a semiconductor region (300) having a top surface [p. 6, lns 6-7, p. 8, lns 20-22; Figs. 2, 3], a source region (121/131) in the semiconductor region [p. 6, lns 15-16, p. 7, ln 3; Figs. 2, 3], a drain region (122/132) in the semiconductor region [p. 6, lns 15-16, p. 7, ln 3; Figs. 2, 3], a channel region (125/135) in the semiconductor region between the source region and the drain region [p. 6, lns 15-16, p. 7, lns 4-6; Figs. 2, 3], and an impurity region (228/238) within the channel region and spaced from the top surface, the impurity region having a first outer boundary that is proximate, but laterally spaced apart from the source region and a second outer boundary proximate, but laterally spaced apart from the drain region. P. 6, lns 18-20, p. 7, lns 7-9; Figs. 2, 3; Figs. 2, 3. It also includes a gate (123/133) overlying the channel region and a gate dielectric (124/134) between the gate and the channel region. P. 6, lns 15-17, p. 7, lns 4-6; Figs. 2, 3.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. 41.37(c)(1)(vi))

***A. First Grounds***

Claims 1, 3, 6, and 7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Serial Number 2002/0074598A1 to Doyle, et al. (hereinafter "*Doyle*").

***B. Second Grounds***

Claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Doyle* in view of U.S. Patent No. 4,069,094 to Shaw (hereinafter "*Shaw*").

***C. Third Grounds***

Claims 4-5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Doyle*.

***D. Fourth Grounds***

Claims 8-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Doyle* in view of U.S. Patent No. 6,759,717 to Sagarwala, et al. (hereinafter "*Sagarwala*").

## ARGUMENT (37 C.F.R. 41.37(c)(1)(vii))

In accordance with the provisions of 37 C.F.R. 41.37(c)(1)(vii), Appellant provides argument and rationale in support of its position of patentability separately for each of the grounds of rejection. However, the common thread of dispute contested by Appellant lies in the application and interpretation of the primary reference, *Doyle*, which forms the basis of each of the grounds of rejection under appeal. Therefore, Appellant provides detailed treatment of this dispute with regard to the First Grounds, and, thereafter, in consideration of the Board's time and, in an effort to refrain from repetitive argument, Appellant will refer back to such detailed treatment for the Second through Fourth Grounds.

### *A. First Grounds*

Claims 1, 3, 6, and 7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by *Doyle*. Claims 3, 6, and 7 each depend from claim 1 and, thus, inherit all limitations from claim 1. The Examiner's rejections will, therefore, be addressed as to claim 1, but each argument for claim 1 would apply equally for claims 3, 6, and 7.

The issue with regard to the Examiner's rejection under 35 U.S.C. § 102(e) is whether *Doyle* discloses "an impurity region within the channel region ...", as required by claim 1. In the Examiner's comments from the Advisory Action, she notes that (1) *Doyle*'s usage of the term "oxidized voids" and other "un-cited" statements in *Doyle* indicate that the voids include at least a portion of an oxide – thus, an impurity region within the channel region; and (2) *Doyle* provides that "oxygen may be implanted" after formation of the device on the substrate, so that even if the implanted oxygen is temporary, there is an intermediate form of the device that still reads on the claims.

#### 1. Oxidized Voids

*Doyle* describes the "oxidized voids" at paragraphs [0036] and [0044] using the same terminology for both. While the Examiner interprets *Doyle*'s use of the phrase "oxidized voids" as describing some kind of oxide formed within or around the voids, Appellant asserts that, in the context used in *Doyle*, the term oxidized void describes the manner in which the voids are

formed. *Doyle* states that oxygen ions may "be used in reaction to alter the internal region of the substrate by way of specific volume or thermal expansion differences (e.g., oxidized voids)." ¶s [0036] & [0044]. Annealing takes place later which causes the voids to actually form in the substrate. ¶ [0038]. Thus, Appellant asserts that "oxidized void" is a term used in *Doyle* to describe the manner in which the voids are formed in the substrate, and not a description of the material make-up of the voids, as asserted by the Examiner. An oxidized void, as described in *Doyle,* is a void that is formed through the oxidation process.

While the Examiner asserts that other language from *Doyle* supports her conclusion, there is, in fact, no other language in *Doyle* that would tend to support that an oxidized void actually means some kind of oxidized substance rather than simply a void formed through oxidation. *Doyle* states that the annealing process begins repairing the substrate material, but that these voids then form as a result. ¶ [0038]. Void here having its commonly understood meaning of a hole or absence of material at that location. *See* ¶ [0034] ("the implanted gaseous substance generally migrates or diffuses of the substrate, leaving behind a void in the substrate"). There is no disclosure in *Doyle* that indicates any oxidized material remains that is related to the oxidized voids or even the surrounding area. Thus, there is no disclosure in *Doyle* that supports the Examiner's contention. As such, a void, whether an oxidized void or otherwise, is not the same as the impurity region required by claim 1. Therefore, claim 1 is patentable over the teachings in *Doyle*.

2. Intermediate Device

The Examiner also asserts that *Doyle* describes an "intermediate product" that reads on claim 1. The Examiner notes that "Doyle states in [0036] that ***oxygen*** may be implanted after formation of the device on the substrate" such that even if the impurity is temporary, it still constitutes an intermediate product that reads on the claims. Advisory Action, continuation sheet. (emphasis added.) In fact, *Doyle* does ***not*** state that oxygen is implanted after formation of the device. The direct language from *Doyle* paragraph [0036] reads, "The ***voids*** of the present invention may be implanted into the substrate before, during, or after the formation of a device on the substrate." ¶ [0036] (emphasis added). The Examiner's mistaken quotation of *Doyle* elicits a misleading conclusion regarding any post-formation operations.

Only one of the examples discussed in *Doyle* describes a process occurring ***after*** device formation. Figures 13-16 show voids being created in the gate of an NMOS device. However, claim 1 requires the impurity region to be in the channel region, which the gate region is not. The fact that a certain result or characteristic ***may*** occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). Therefore, there is no teaching in *Doyle* that describes any impurity region within the channel in a post-formation process, which would constitute the "intermediate" device asserted by the Examiner. Without any teaching of this alleged intermediate device, the Examiner's reasoning is unsupported by *Doyle*'s disclosure.

3. Doyle Does Not Teach the Identical Claimed Invention

"A claim is anticipated ***only if*** each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (emphasis added). Moreover, "[t]he ***identical invention*** must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989) (emphasis added). Based on the teachings of *Doyle*, the identical invention is not taught in complete detail as is described and required in claim 1 and each of the claims that depend from claim 1. The voids formed through oxidation of the implanted gasses in *Doyle* are not the identical structure to the impurity region, required by claim 1. Accordingly, Appellant respectfully requests that the rejection of claims 1, 3, 6, and 7 be overruled.

***B. Second Grounds***

Claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Doyle* in view of *Shaw*.

Claim 2 depends from and inherits all limitations from claim 1. While the Examiner admits that *Doyle* does not teach that the semiconductor region comprises monocrystalline

silicon and offers *Shaw* to cure this deficiency, the failure of *Doyle* to teach an impurity region within the channel, as required by claim 1, and as argued fully above, means that *Doyle* simply does not teach or suggest each and every limitation of claim 2. *Shaw* does not teach such limitation, nor does the Examiner rely on *Shaw* to teach an impurity region within the channel. Thus, the combination of *Doyle* and *Shaw* also does not teach each and every limitation of claim 2. Therefore, based on the arguments above, Appellant respectfully requests that the rejection of claim 2 be overruled.

***C. Third Grounds***

Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Doyle.*

Claims 4 and 5 each depend from and inherit all limitations from claim 1. The Examiner admits that *Doyle* does not teach the relative distances of the impurity region from the top surface or that silicon dioxide is used in the gate dielectric and asserts that such limitations would be obvious to one of ordinary skill in the art. However, the failure of *Doyle* to teach an impurity region within the channel, as required by claim 1, and as argued fully above, means that *Doyle* simply does not teach or suggest each and every limitation of claims 4 and 5. Therefore, based on the arguments above, Appellant respectfully requests that the rejection of claims 4 and 5 be overruled.

***D. Fourth Grounds***

Claims 8-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Doyle.* In view of *Sagarwala.*

Claims 8-12 each depend from and inherit all limitations from claim 1. While the Examiner admits that *Doyle* does not teach sidewall spacers, lightly-doped source/drain regions, or a second transistor, she offers *Sagarwala* to cure these deficiencies. However, *Doyle* fails to teach an impurity region within the channel, as required by claim 1, and as argued fully above. *Sagarwala* does not teach such limitation, nor does the Examiner rely on *Sagarwala* for such limitation. Therefore, the combination of *Doyle* and *Sagarwala* simply does not teach or suggest

each and every limitation of claims 8-12. Therefore, based on the arguments above, Appellant respectfully requests that the rejection of claims 8-12 be overruled.

## CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

## EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted, hence no Evidence Appendix is included.

## RELATED PROCEEDINGS

No related proceedings are referenced above, hence no Related Proceedings Appendix is included.

Respectfully submitted,

12/24/07
Date

Thomas J. Meaney
Attorney for Appellant
Reg. No. 41,990

SLATER & MATSIL, L.L.P.
17950 Preston Rd., Suite 1000
Dallas, Texas 75252
Tel.: 972-732-1001
Fax: 972-732-9218

## CLAIMS APPENDIX

1. (Previously Presented) A transistor device comprising:

a semiconductor region having a top surface;

a source region in the semiconductor region;

a drain region in the semiconductor region;

a channel region in the semiconductor region between the source region and the drain region;

an impurity region within the channel region and spaced from the top surface, the impurity region having a first outer boundary that is proximate, but laterally spaced apart from the source region and a second outer boundary proximate, but laterally spaced apart from the drain region;

a gate overlying the channel region; and

a gate dielectric between the gate and the channel region.

2. (Original) The device of claim 1 wherein the semiconductor region comprises a region of monocrystalline silicon.

3. (Original) The device of claim 2 wherein the semiconductor region comprises a silicon substrate.

4. (Original) The device of claim 1 wherein the source and drain regions extend into the semiconductor region a first distance, and wherein the impurity region is spaced from the top surface by a distance less than the first distance.

5. (Original) The device of claim 1 wherein the gate dielectric comprises silicon dioxide.

6. (Original) The device of claim 1 wherein the impurity region comprises a region of an implanted oxygen bearing species in the channel region.

7. (Original) The device of claim 1 wherein the channel region comprises a strained channel region.

8. (Original) The device of claim 1 and further comprising:

a first sidewall spacer adjacent a first sidewall of the gate;

a second sidewall spacer adjacent a second sidewall of the gate;

a lightly doped drain region within the semiconductor region adjacent the drain region, the lightly doped drain region disposed beneath the first sidewall; and

a lightly doped source region within the semiconductor region adjacent the source region, the lightly doped source region disposed beneath the second sidewall.

9. (Original) The device of claim 1 and further comprising a second transistor, the second transistor including:

a second source region in the semiconductor region;

a second drain region in the semiconductor region;

a second channel region in the semiconductor region between the second source region and the second drain region;

a second gate overlying the channel region; and

a second gate dielectric between the gate and the channel region.

10. (Previously Presented) The device of claim 9 further comprising a second impurity region within the second channel region and spaced from the top surface, the second impurity region having a first outer boundary proximate, but laterally spaced apart from the source region and a second outer boundary that is proximate, but laterally spaced apart from the drain region.

11. (Original) The device of claim 9 wherein the second transistor does not include an impurity region within the second channel region.

12. (Original) The device of claim 9 wherein the second transistor device comprises an n-channel transistor.